Referring to Figure 2, the transmitter regulator 200 receives an input voltage V_{in} on the order of 5.5 volts, or any other desired input voltage. The voltage input, designated 202 is used as the supply for the drain of a voltage switch 204, represented as a pnp transistor Q2, such as a transistor designated 263XCG133, available from Solitron Corporation.

The voltage input 202 is supplied via voltage stabilizing and filter components represented in the exemplary Figure 2 embodiment as a Zener diode 206, and parallel capacitors 208 and 210. The voltage input 202 is also supplied as the input voltage to a voltage regulator chip 212, such as the chip designated LT1573 available from Linear Technology, Inc. The voltage regulator chip 212 also includes a shutdown input 216, a latch input 218, and a ground connection 220.

Outputs of the voltage regulator chip 212 include a drive output 222 for driving the base of the voltage switch 204 via a voltage divider comprised of resistors 224 and 226. An additional output of the voltage regulator chip is designated as the voltage output, V_{out} , which is connected to the collector of the voltage switch 204. The voltage regulator chip 212 includes a comparison output 230. The comparison output 230 is supplied to the collector of the voltage switch 204 via a resistor 232, a resistor 234 and a capacitor 236. The compare output compares a feedback signal from the regulator output with the V_{out} voltage to monitor collector current and to adjust a setpoint. The feedback is received via a feedback input 232 connected to the collector of the voltage switch 204, via resistor 238, adjustable resistor 240, and capacitors 242 and 244. The adjustable resistor permits adjustment of the drain bias voltage output from the regulator. The output from the collector of the voltage switch 204 is, in the exemplary embodiment illustrated, a five volt DC bias 246.

To protect the circuit against high current fluctuations, the transmitter regulator is configured with a protective means, whereby the voltage regulator chip 212 cannot operate unless a voltage V_x at a node 248 is sufficiently negative. The shutdown input 216 of the voltage regulator chip 212 is connected to a node between resistor 250 and diode 252. The diode 252 is connected to the collector of a transistor 254, such as a

transistor chip 2N3904 available from Solitron Corp. The base of this transistor is grounded, and the drain is connected via a resistor 256 to the node 248.

The node 248 corresponds to the output of a negative voltage regulator, such as the regulator LT1175 available from Linear Technology, Inc. The negative voltage regulator 258 receives an input voltage on the order of -6 volts, or less, supplied via a reverse biased diode 260, a resistor 262, and a voltage stabilizing filter circuit which includes a Zener diode 264, capacitor 266 and capacitor 268 connected in parallel.

The desired value of V_x at node 248 can be adjusted via a divider network that includes a resistor 270 and an adjustable resistor 272. The voltage V_x is supplied to a second output of the transmitter regulator to provide a gate bias on the order of -3 volts DC, at the output 274. The voltage V_x is supplied to the regulator output 274 via a filter which includes capacitor 276, a capacitor 278, and via a voltage divider network which includes resistors 280 and 282. Exemplary component values for each of the components shown in Figure 2 are illustrated.

In operation, when the proper voltage is output from the negative voltage regulator 258 to the node 248, a current path can be established from the input 202 to the node 248, such that the shutdown input 216 of the voltage regulator chip 212 remains inactive. However, if the voltage at node 248 rises above a predetermined threshold established by the user such that it becomes at or near zero, or positive, current will not flow from the voltage input 202 to the node 248. Rather, current can flow from the voltage input 202 into the shutdown input 216 of the voltage regulator 212, thereby causing the voltage regulator chip 212 to inhibit a drain bias voltage at the output 246 of the transmitter regulator 200.

In operation, the gate voltage at the output 274 is controlled to be between -1 volt and -3 volts, depending on the adjustments made to adjustable resistor 272, to control current throughout the transmitter. When a proper negative voltage appears at the node 248 (and thus, the output 274), then the voltage regulator 212 will be enabled to provide the 5 volt drain bias at the output 246. Similar transmitter regulators can be included for the other components of the Figure 1 transmitter as discussed previously.

Having described an exemplary embodiment of a transmitter and transmitter regulator, reference is made to Figure 3 wherein an exemplary receiver in accordance with the present invention is illustrated. The Figure 3 receiver 300 constitutes a means for reception of information, and includes means for performing at least one of modulating and demodulating information signals. Because Figure 3 illustrates a receiver portion of a transceiver, a demodulating means is illustrated which includes a data input means and a data processing means. Like the transmitter, the Figure 3 receiver is configured using at least one monolithic millimeter wave integrated circuit. For example, as with the transmitter, amplifiers and frequency multipliers can be available monolithic millimeter wave integrated circuits, as can a demodulator. Alternately, all components can be configured using MMICs. In addition, all components of the receiver, (including an antenna, the local oscillator, any voltage regulator and so forth), can be configured on a single substrate.

The data input means includes an information input channel and a local oscillator input channel. The information input channel includes the radio frequency input 302, a microstrip line to coaxial connector 304, an amplifier 306, and a bandpass filter 308. An output of the information input channel is supplied to a demodulator, or converter (i.e., mixer) 310. The demodulator 310 can, for example, be a downconverter which produces an output with a frequency that is lower than the frequencies of either input to the downconverter, or can be any other type of demodulator.

The demodulator 310 also receives the output of the local oscillator input channel. The local oscillator input channel of the Figure 3 receiver is configured identically to that of the local oscillator input channel illustrated in the Figure 1 embodiment of a transmitter. More particularly, the local oscillator input channel includes the local oscillator input 312, a microstrip line to coaxial connector 316, an amplifier 318, a frequency multiplier 320 and a bandpass filter 322. The demodulator 310, like that of the Figure 1 transmitter, produces an output which corresponds to both the sum and the differences of frequencies f_1 and f_2 associated with the information and local oscillator input channels, with the difference being output from the demodulator